REMARKS/ARGUMENTS

The Office Action mailed July 16, 2007 has been received and the Examiner's comments carefully reviewed. Claims 2-11 and 44-53 are rejected. Claims 2, 44 and 50 have been amended. For at least the following reasons, Applicants respectfully submit that the pending claims are in condition for allowance.

Claim Rejections

Claims 2-5, 7-10, 44-51 were rejected under 35 U.S.C. 103(a) as being unpatentable by Lorang et al in view of Chadwick (US 5,168,271). Claims 6,11,52,53 were rejected under 35 U.S.C. 103(a) as being unpatentable by Lorang in view of Chadwick and further in view of Cameron (US 2002/0051499). The Applicants respectfully disagree but have amended the claims to more clearly define the invention.

As amended, Claim 2 recites in part "a packet assembler coupled to said encoder and to the first interface such that the packet assembler receives input from the data encoder when transmitting at a first transmission speed and the packet assembler receives input from the first interface when transmitting at a second transmission speed, such that first encoder is bypassed when transmitting at the second transmission speed." In contrast, Chadwick discloses an interleaver configured to receive input only from an encoder, but not directly from a traffic information processor.

For example, the Office Action states "means for encoding data for transmission (see Fig. 10 regarding the TX path, protocol control 354 and protocol processor 356 which would

implicitly disclose an encoder as disclosed by Chadwick in Fig. 2)" (Office Action, page 3) and "the 'interleaver 116' and the 'frame+sync. 120' in Fig. 2 of Chadwick would read on the 'packet assembler' in accordance with the specification description an encoder as disclosed by Chadwick in Fig. 2)" (Office Action, page 5).

Chadwick, however, teaches an interleaver configured to receive input only from an encoder, but not directly from a traffic information processor. "Referring now to FIG. 2, there is shown a block diagram of the STIC modulator 110... Digital data representing traffic information is coupled from the traffic information processor 70 to the encoder 112 by the data coupling line 72. Encoder 112 encodes the digital data received from processor 70 with a forward error correction code...The encoded data from encoder 112 is coupled to the interleaver 116 by the data coupling line 114" (Chadwick, col. 4, lines 36-53). As explained by Chadwick, data is transmitted between blocks through coupling lines.

Chadwick teaches two coupling lines: one (coupling line 72) that connects the traffic information processor 72 to the encoder 112, and another (coupling line 114) that connect the encoder 112 to the interleaver 116. Chadwick does not teach a coupling line that connects the interleaver 116 directly to the traffic information processor. Accordingly, ***Chadwick does not teach a packet assembler coupled to said encoder and to the first interface***, as is recited by Claim 2.

Further, as Chadwick does not teach a coupling line that connects the interleaver 116 directly to the traffic information processor, the system of ***Chadwick cannot bypass the encoder***. Further still, Chadwick does not teach that the encoder may be bypassed to reduce encoding time

in order to transmit ***at two transmission speeds***. Since Chadwick does not teach a packet assembler coupled to said encoder and to the first interface such that the packet assembler receives input from the data encoder when transmitting at a first transmission speed and the packet assembler receives input from the first interface when transmitting at a second transmission speed, such that first encoder is bypassed when transmitting at the second transmission speed, Claim 2 is proposed to be allowable. Claims 3-11 are proposed to be allowable as they depend from a valid base claim.

As amended, Claim 44 recites in part "means for assembling packets from data provided by the data source when transmitting at a first transmission speed and from data provided by the data source when transmitting at a second transmission speed, such that the means for assembling packets is bypassed when transmitting at a second transmission speed." For at least the reasons presented above, Claim 44 is proposed to be allowable. Claims 45-49 are proposed to be allowable as they depend from a valid base claim.

As amended, Claim 50 recites in part "an assembler that is coupled to the encoder and to the interface such that the assembler receives input from the encoder when transmitting at a first transmission speed and the assembler receives input from the interface when transmitting at a second transmission speed, wherein the assembler is arranged to interleave the received input into data segments, add correlation information to the data segments, and convert the data segments into a bit stream." For at least the reasons presented above, Claim 50 is proposed to be allowable. Claims 51-53 are proposed to be allowable as they depend from a valid base claim.

Conclusion

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicants at the telephone number provided below.

Respectfully submitted,

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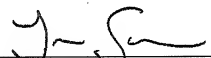

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